IFW

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Teck Kheng Lee

Serial No.: 10/829,603

Filed: April 22, 2004

For: METHODS FOR ASSEMBLY AND PACKAGING OF FLIP CHIP CONFIGURED DICE WITH INTERPOSER

Confirmation No.: 6862

Examiner: Unknown

Group Art Unit: 2823

Attorney Docket No.: 2269-4974.2US
(00-0693.02/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

November 15, 2004
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 or PTO/SB/08 be considered by the Examiner and made of record. Copies of U.S. patents are not being submitted pursuant to M.P.E.P. 609 III A(2). Copies of foreign patent documents and non-patent literature are enclosed pursuant to 37 C.F.R. § 1.98(a)(2).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicant herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

U.S. Patent No.	Publication Date	Patentee
US - 3,239,496	03/1966	Jursich
US - 4,074,342	02/1978	Honn et al.
US - 4,818,728	04/1989	Rai et al.
US - 5,148,265	09/1992	Khandros
US - 5,346,861	09/1994	Khandros
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US - 5,468,681	11/1995	Pasch
US - 5,489,804	02/1996	Pasch
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US - 6,177,723	01/2001	Eng et al.
US - 6,217,343	04/2001	Okuno
US - 6,222,265	04/2001	Akram et al.

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Foreign Patent Documents

Document No.	Publication Date	Patentee
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EP 1009027	06/2000	Okuno
KR 2001054744	07/2001	Choi et al. (English Abstract)

Other Documents

AL-SARAWI et al., AA review of 3-D packaging technology,@ Components, Packaging, and Manufacturing Technology, Part B: IEEE Transactions on Advanced Packaging, Vol 21, Issue 1, Feb. 1998, pp. 2-14.

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FERRANDO et al., A Industrial approach of a flip-chip method using the stud-bumps with a non-conductive paste,@ Adhesive Joining and Coating Technology in Electronics Manufacturing, 2000. Proceedings. 4th International Conference on, 18-21, June 2000, pp. 205-211.

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GEISSINGER et al., A Tape Based CSP Package Supports Fine Pitch Wirebonding,@ Electronics Manufacturing Technology Symposium, 2002, IEMT 2002, 27th Annual IEEE/SEMI International, 17-18 July 2002, pp. 41-452.

HATANAKA, H., A Packaging processes using flip chip bonder and future directions of technology development,@ Electronics Packaging Technology Conference, 2002. 4th, 10-12, Dec. 2002, pp. 434-439.

HAUG et al., A Low-Cost Direct Chip Attach: Comparison of SMD Compatible FC Soldering with Anisotropically Conductive Adhesive FC Bonding,@ IEEE Transactions on Electronics Packaging Manufacturing, Vol. 23, No. 1, Jan 2000, pp. 12-18.

KLOESER et al., A Fine Pitch Stencil Printing of Sn/Pb and Lead Free Solders for Flip Chip Technology,@ IEEE Transactions of CPMT - Part C, vol. 21, No. 1, 1998, pp. 41-49.

LEE et al., A Enhancement of Moisture Sensitivity Performance of a FBGA,@ Proceedings of International Symposium on Electronic Materials & Packaging, 2000, pp. 470-475.

Other Documents

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LYONS et al., "A New Approach to Using Anisotropically Conductive Adhesives for Flip-Chip Assembly, Part A, " *IEEE Transactions on Components, Packaging, and Manufacturing Technology,* Vol. 19, Issue 1, March 1996, pp. 5-11.

TEO et al., "Enhancing Moisture Resistance of PBGA," *Electronic Components and Technology Conference,* 1988. 48th IEEE, 25-28 May 1998, pp. 930-935.

TEUTSCH et al, "Wafer Level CSP using Low Cost Electroless Redistribution Layer," *Electronic Components and Technology Conference*, 2000. 2000 Proceedings. 50th, 21-24 May 2000, pp. Pages: 107-113.

"The 2003 International Technology Roadmap for Semiconductor: Assembly and Packaging."

TSUI et al., "Pad redistribution technology for flip chip applications," *Electronic Components and Technology Conference*, 1998. 48th IEEE, 25-28 May 1998, pp. 1098-1102.

XIAO et al., "Reliability study and failure analysis of fine pitch solder-bumped flip chip on low-cost flexible substrate without using stiffener," IEEE, 2002. Proceedings 52nd, 28-31 May 2002, pp. 112-118.

Applicant offers to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits.

Respectfully submitted,

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Date: November 15, 2004
TNB/lmh:ljb

Enclosures: Form PTO-1449 or PTO/SB/08
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 4

Complete if Known	
Application Number	10/829,603
Filing Date	April 22, 2004
First Named Inventor	Teck Kheng Lee
Group Art Unit	2823
Examiner Name	Unknown
Attorney Docket Number	2269-4974.2US (00-0693.02/US)

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	Document Number: Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-3,239,496	03/1966	Jursich	
		US- 4,074,342	02/1978	Honn et al.	
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		US- 5,468,681	11/1995	Pasch	
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		KR 2001054744	07/2001	Choi et al. (English Abstract)		x

Examiner Signature		Date Considered	

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Sheet 3 of 4

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NON PATENT LITERATURE DOCUMENTS

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		AL-SARAWI et al., AA review of 3-D packaging technology,@ Components, Packaging, and Manufacturing Technology, Part B: IEEE Transactions on Advanced Packaging, Vol 21, Issue 1, Feb. 1998, pp. 2-14.	
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